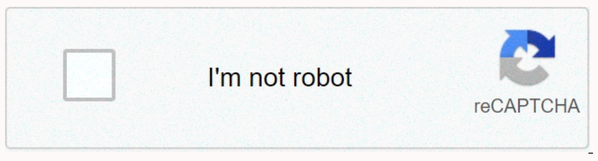

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Implementation using nand gates only pdf

The three fundamental logical functions (at least for binary logic) are AND, OR, and NOT. As it happens, if you have a collection of nand portals you are able to all of them. A 2-inch NAND gateway with the two inputs tied together, or one input tied low, is a converter and does not perform NO. In addition, DeMorgan's Theorem tells you that, with inverted input, a NAND gateway functionally becomes an OR gateway. So you can do everything with only nand gates. Similarly, DeMorgan's Theorem applies equally to NOR gateways – reverse inputs and become AND portal. Usually, a logic IC will either use the formula as a key building block, and repeat the gates as needed. The classic 7400 family and its bipolar descendants used an NPN multi-transmitter transistor that worked just fine as a NAND gateway. Holding on to a single building block simplified chip design back when it was all done manually, and allowed for simple tweaking process where using multiple portal types would have made life difficult. This article is about NAND Logic in the sense of building other logic portals using only NAND portals. For NAND Gates, see NAND portal. For NAND in the purely logical sense, see Logical NAND. For logic portals in general, see Logic Portal. This article is based largely or entirely on a single source. A discussion can be found on the discussion page. Help improve this article by entering references to additional sources. Find sources: NAND logic - news · newspapers · books · scholar · JSTOR (July 2012) NAND Boolean has the status of functional completeness. This means that any binary expression can be re-expressed with an equivalent expression using only NAND functions. For example, NOT(x) can be expressed equally as NAND(x,x). In the field of digital electronic circuits, this means that we can apply any Boolean function using only NAND gateways. The mathematical proof of this was published by Henry M. Sheffer in 1913 in the transactions of the American Mathematical Society (Sheffer 1913). A similar case applies to the NOR function, and this is referred to as nor logic. NAND Main Article: NAND Portal A NAND Portal is an inverted and portal. It has the following truth table: Q = NAND B Truth Input Table A Input B Output Q 0 0 1 1 1 0 1 1 1 1 Making other gateways using nand gates A NAND gateway is a universal gateway, which means that any other gateway can be represented as a combination of NAND gateways. DO NOT See also: NO gateway IS NOT done by joining the inputs of a NAND portal together. Since a portal is equivalent to a PORTAL AND followed by a NOT gateway, joining the entrances of a NAND gateway leaves only the PORTAL NOT. Desired NOT Portal NAND Construction Q = NOT(A) = A NAND A Table Truth Input A Output Q 0 1 1 0 AND See also: AND Gate A gateway and is done by reversing the output of one gate, as shown below. Desired and Portal NAND Construction Q = A AND B = (A NAND B) NAND (A NAND B) Truth Input Table A Input B Output Q 0 0 0 0 0 1 1 1 1 1 Or See also: Or portal If the truth table for a NAND portal is examined or by applying de Morgan laws, it can see that if any of the inputs are 0 , then the output will be 1. To be an OR gateway, however, the output must be 1 if any input is 1. Therefore, if the inputs are inverted, any high input will cause a high output. Desired or portal NAND Construction Q = A OR B = (A NAND A) NAND (BAND B) Truth Input Panel A Input B Output Q 0 0 0 0 1 1 1 1 1 1 NOR See also: NOR gateway NOR is not a gateway Or with inverted output. The output is high when neither entrance A nor entrance B is high. Desired NOR Gate NAND Construction Q = A NOR B = [(A NAND A) NAND (B NAND B)] NAND [(A NAND A) NAND (BAND B)] Truth table image Input A Input B Output Q 0 0 1 0 1 1 0 0 0 XOR See also: XOR Gate A XOR gateway is made by connecting four NAND gateways as shown below. This construction entails a delay of dissemination three times that of a single NAND portal. Desired xor gateway NAND Construction Q = A XOR B = [A NAND (A NAND B)] NAND [BAND (A NAND B)] Truth table input A input B Output Q 0 0 0 0 1 1 1 1 1 1 0 Alternatively, An XOR gateway is made by looking at the normal format A - B , + A , B { \displaystyle A\cdot {\overline {B}+{\overline {A}}\cdot B} , noting by de Morgan law that a NAND portal is an inverted entrance or gateway. This structure uses five gates instead of four. Desired Nand Gate Construction Q = A XOR B = [B NAND (A NAND A)] NAND [A NAND (B NAND B)] XNOR See also: Gate XNOR An XNOR portal is made by looking at the discunctive normal format A ☐ B + A' ☐ B' {\displaystyle A\cdot B+{\overline {A}\cdot {\overline {B}}} , noting by de Morgan law that a NAND gateway is a gateway or inverted input or. This construction entails a delay of dissemination three times that of a single NAND portal and uses five gates. Desired XNOR Gate NAND Construction Q = A XNOR B = [(A NAND A) NAND (B NAND B) NAND (A NAND B) Input B Output Q 0 0 1 0 1 1 1 1 1 Alternatively, the 4-gate version of the XOR gateway can be used with a converter. This build has a propagation delay four times (instead of three times) that of a single NAND portal. Desired NAND Gateway Construction Q = A XNOR B = { [A NAND (A NAND B)] NAND [BAND (A NAND B) } NAND { [A NAND (A NAND B)]] MUX A multiplexer or MUX gate is a three-input gateway that uses one of the inputs, called a bit selector, to select one of the other two the data called, bit of data named and extracts only the selected bit of data. [1] Desired mux gateway NAND construction Q = [A and not (s)] or (B and s) = [a NAND (S NAND S)] NAND (BAND S) Input Truth Table A Input B Select Output Q Q 0 0 0 0 1 0 0 1 0 0 1 1 1 0 1 0 0 1 1 1 1 1 1 0 1 0 1 0 1 0 0 0 0 1 0 1 0 1 0 1 1 1 DEMUX An amulessor performs the opposite function of a multiplex: It needs a single input and channels it to one of two possible outputs according to a bit selector that determines which output to choose. [1] Desired DEMUX NAND Gate Construction Truth Table Input Select Exit Output B 0 0 0 0 0 1 1 0 0 1 0 0 1 1 0 1 1 See also Stroke Sheffer - another name NOR logic. Like NAND gateways, nor gates are also universal gateways. Functional completeness External connections TTL NAND and and gateways - All about the circuits Steps to extract XOR from the NAND portal. References ^ a b Nisan, N. & Schocken, S., 2005. In: From NAND to Tetris: Building a modern computer from the earliest beginnings. s.l.: Mit Press, p. 20. Available on: 2001.pdf Archived 2017-01-10 at Wayback Machine Lancaster, Don (1974). TTL Cookbook (1st cm). Indianapolis, IN: Howard C Sams. p. 126–135. ISBN 0-672-21035-5. Sheffer, H.M. (1913), A total of five independent posts for boolean algebra, with application to reasonable constants, Transactions of the American Mathematical Society, 14: 481-488, doi:10.2307/1988701, JSTOR 1988701 Retrieved from In this instructable, we will build NO, and, or gates using nand gates only. In the next steps, we will enter the binary algebra and draw nand-based configurations for the desired portals. NAND and NOR gateways are universal gateways, and so any binary mode can be built using either NAND or NOR portals only. Here are two links to the instructions covering the basic principles of digital logic portals:1. Digital logic portals (part 1)2. Digital Logic Gates (Part 2) Please feel free to post any questions about what is guided in the comments section below. Enjoy! Boolean algebra is a branch of mathematical logic where variables are either true (1) or false (0). To construct NO, AND, or gates from nand gates only, we must be familiar with the following laws boolean algebra:1. Law 2. Idemponcy (Idempotent) Act 3. DeMorgan Law The three laws are explained in Figure 1.Also, we are going to use the 74LS00 IC chip to manufacture nand-based derivative configurations on a bread board, in order to confirm the results. Note that the pin #7 is connected ground and the Pin #14 is connected to the power voltage (5V). Parts Required: Breadboard 9V Battery Battery Connection Battery 5V Regulator IC Chip: 74LS00 An LED (any color) A 330 Ohm Resistance Cables as NAND-based production of the NOT portal is shown in Figure 1. It is also important to note that the entrances to the NAND gates are connected to each other. the same entrance. In Figure 2 & 3, the NAND-based configuration emerged, the two possible inputs, zero and one, were tested, and the results Observed. Thus, from the results, we can conclude that the introduction of the same input through a NAND 2 input gateway will result in the compliment of the input. a logical denial that matches the truth table of a NOT gateway shown in Figure 4 is applied. The output of the NAND-based AND portal is shown in Figure 1. For the bread board portion of this step, the blue cable represents input 1 (A), cable 2 represents input 2 (B), and the LED represents the final output. Finally, from the results, we can conclude that the derived configuration of nand gateways is correct and is indeed equivalent to a PORTAL AND because the results match the truth table of the AND portal shown in Figure 6. The output of the NAND-based OR gateway is shown in Figure 1. For the bread board portion of this step, the blue cable represents input 1 (A), cable 2 represents input 2 (B), and the LED represents the final output. Finally, from the results, we can conclude that the derived configuration of nand gateways is correct and is indeed equivalent to an OR gateway, because the results match the TRUTH table of the OR portal shown in Figure 6. 6.

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