# Asic and fpga design flows pdf

Before we start discussing what is and what is fappa, we will first learn about the basics that a VLSI should know. Moore's Law: Moore's Law Observes that every two years the number of production starts in a densely connected circuit doubles. It is constantly driving vlsi industry and the results of this law are the latest technical nod (i.e. 28nm, 14nm, 12nm, 10nm, 7nm, 5nm). The technology depends on the length of the eclipse gate channel. So, if the length of the gate channel is 10nm then we call it as 10nm technology nod. Integrated Circuit: An integrated circuit or a connected circuit (also called as an IC, a chip, or a microchip) is a set of electronic circuits on a small flat piece (or chip) that usually goes to the sercan of semi-material. We have 3 types of application based IC. They are ASIC (Specific Integrated Circuit), Fipga (Field-Kermadish Gate Sarni) and SoC (Chip-on-System) ASIC: ASIC means the application-specific merger circuit. It is a device that is created for a specific purpose or functionality. They contain only one functionality in them and through the life of the chip, it can only perform this task. For example, the CPU in your phone is an ASIC. This means working as a CPU for his entire life. Its logic function cannot be turned into anything else because its digital circuit is made of permanently attached doors and flips over the philips. The difference in the case is that the resultcircuit is permanently developed in the silicon while the circuit in the fappa is made by the circuit setting attached to a number of blocks. Fipga: Fipga means field-kermades gate row. It may be the field program to work according to the required design. This means that it could act as a micro processor or graphics card, or both at the same time. The design on the fappa is usually produced using hardware-defined languages such as the wand and the verlog. The FPIs are made up of number of order logic blocks (CLB) and are connected with The Karmadis Interconnects. CLB are made mainly from the eye-top tables (Lot), Moltapalyars and Philip Philips. They can apply complex logic functions. In addition to CLB, and the route, many of the fifga also contains hard-scented blocks dedicated to different functions such as RAM, DSP blocks, external memory controllers, PLL etc. These are important in competition with the leading hardware blocks ASIC. SoC: SoC means the system on the chip. It consists of one or more microprocessors (cores) or microprocessors or DSp cores along with all other Ips (intellectually owned) such as memory IP, alien IP etc. In other terms, if one or more processors are involved, then it is called an ASIC. Flow of the fappa: 1. Design entry: Design can be registered using two methods.

One is through Another hardware description is through language (the language). Tools to reduce these skimtoctok skimor or to reduce the risk with converting to skimtalk. Generally, the maximum deal with complex systems is better for a design, to opt out for the risk-reduction, a fast, language-based process in which you need to design in low-level hardware, while Schematox is a good choice for someone who has a good choice because it is the whole system The skimtalk-based approach goes to work better for lower levels or smaller designs while the risk for complex design is better to go with the com-based approach. 2. Recipe: As the design code we have listed is in the form of, it needs to be converted into a real circuit that we want to implement. It is done by recipe tools such as vivado etc. This behavior code converts the door level to the netlist where the entire circuit will be represented in the form of doors, philip sands and shards. The connection between them is also shown in a netlist. This process starts with a check when you feed into your risk-based design. Then it is accelerated to implement it faster than desired by reducing logic, eliminating excessive logic, and reducing the size of the design. The last step is to map the technology by attaching to the design of the injection, indicating the time attached, and designing netlists that are later preserved. 3. Implementation: This is the stage where your design configuration will be determined and consists of three stages: translation, map, and location & route. The tools used in this phase are provided by Fappa Vendors because they know best how to translate an unrelated netlist into a fappa. The first step for the tool is to collect all the obstacles that are set by the user in conjunction with the netlist files. These obstacles can be about the assignment and position of the pins, such as the maximum delay or time of the clock input period. The tool is then being used to actually tap the implementation of the implementation by comparing the specific resource requirements in files for available resources. The circuit is divided into logical blocks or elements in the form of sub-blocks. As a result, your entire design is placed in specific logic blocks and is determined in the fappa. The next step is to connect and route all signals accordingto all the signals with the obstacles set by the user between all logic blocks and i/O blocks. 4. Program Fappa: The last step in the process is to finally map out and fully load the route design into the fappa. Because of this, you'll need to create a little stream file and it'll be thrown on to the fappa board using this little stream file flash programmer device. When you run your fappa board, your design functionality is greatly lost. It's the whole process for the fappa-based design. me too There is a check that is done at every level. Behavior is done at the level of the design entry, the functional design is done at the level of post-post and time-consuming process. ASIC Flow: 1. Details: Details for products are submitted from the market or customer's needs. This description also includes that the product should contain all the features etc. These are usually collected by marketing people. 2. Architecture Design: Architecture design consists of all the blocks that are designed and how they are attached to the design. They come with a block diagram which includes all the above details based on. This architecture team will estimate the area of the block, how much power is needed and cost for Design 3. RTL Design: RTL design is developed using risk-reduction. It is designed based on the design of architecture. It is written in the verlog or the vedel. This code tells you about how data is transferred between different components in design. 4. RTL Verification: Advanced design is done at this stage. Test trials will be designed to check the design functionality and if any problems are found in the design, it is to modify it and launch the new RTL to the designer. Confirmation itself is 60% of the total life time of chip development. This stage is very important as the design is tested for its functionality. No bugs got post-routeing right and even difficult to build the post we can't design right. So this is a very important part of a quiet development cycle. 5. Recipe: This is an act of converting the RTL code to the gate level netlist. RTL is the independent technology designed to verify. The design in the process of the recipe is converted into a technology dependency. This is a 3-step process. Translation: RTL code is changed to bolin expression. Correction: Boleyn expression is customized by map and reformation methods of THE POS: it is converted into a gate based on bolin expression technology and creates gate level netlist. There are RTL codes for the recipe, SDC and. Selected files. The results generated after the recipe are netlist and the door level. SDC files. 6. Door level simulators: Door level design is used to promote confidence about the implementation of a design and can help to confirm dynamic circuit behavior, which cannot be verified correctly by the static methods. It is running after the RTL code and is handled in the gate level netlist. The gate level is increasing in the cross-exposure analysis ranges and is being used due to low power problems, complex time checking at 40nm and below, designed for test (DFT) on the door level and low power protections For DFT, the door level netlist is prepared after scan chains are put . Often used to determine whether scan chains are correct 7. Designed for Testbalty: Designed for Tsebalty (DFT) is a technique that provides a design facility for post-production testing to become. At this stage we have put additional logic along with the design logic during the processing process which helps to post the production process. DFT post will make testing easier in the production process. At this stage an ATPG (automatic test pattern generator) will create the file. 8. Floorplan: The process of determining the location of the floorplan macro, the power grid generation and the location of I/O. It is the process of placing blocks/macro in a chip/core area by determining the routes between them. It determines the size of the die and makes wire tracks to determine the location of the standard cells. It makes power tracks and defines the pg connection. It also determines the location of the in/O, pin/pad. 9. Location Determination: Location determination is the process of automatically assigning the correct position to the standard cells on the chip with no overlap. The standard cells will be placed almost inside by the outside global space. The standard cells by detailed space will take place in the rows of the site (to determine this). In the deployment phase we do check the price of the sheep by GRC maps. 10. Clock Tree Recipes (CTS): At this stage we made the clock tree using invertors and buffers. The chip clock is essential for Philip Philips in the signal, to give the clock signal from the clock we made the clock tree. It is a process of balancing the clock to meet the time and power to reduce and to reduce the delay of multiple enhancements. 11. Rotation: Macro before the routestage, standard cells, clocks, in/o port are logical connections. At this stage we are physically attached to all cells with metal plates. 1) Global Routed 2) Detailed route. Global rating will tell which signal which metal curtain is used. There are all logical connections before detailed route. The detailed route is made in physical connection. 12. Sagnov & Build: After the physical order of the chip is completed. All tests in the Sagnonov phase are done to check the quality and performance of the layout before the tapuot. The design is then changed to the GDS II file. We're quiet by GDS II file information. Total design is turned into chip by the manufacturers' process. 13. Post-Silicon Authentication: Post-Silicon Authentication is used to detect and resolve bugs in connected circuits and systems after being developed. Post-silicon authentication includes one or more ready chips to verify the correct behavior on the original application environment specific operating conditions. The goal is to ensure that no bugs escape into the field. If there is a design error, we will re-modify the design If there are no errors then the chip will go to packing. 14. Chip: Finally we get the chip we need which will be prepared in bulk. If we use this process to produce only 1 chip, then it costs far more than the actual chip price after production. If we produce chips in bulk then we can save the silicon wofer to produce more chips with a wof and the cost of production for each chip will be lower than the cost for which it has been sold. Sell.