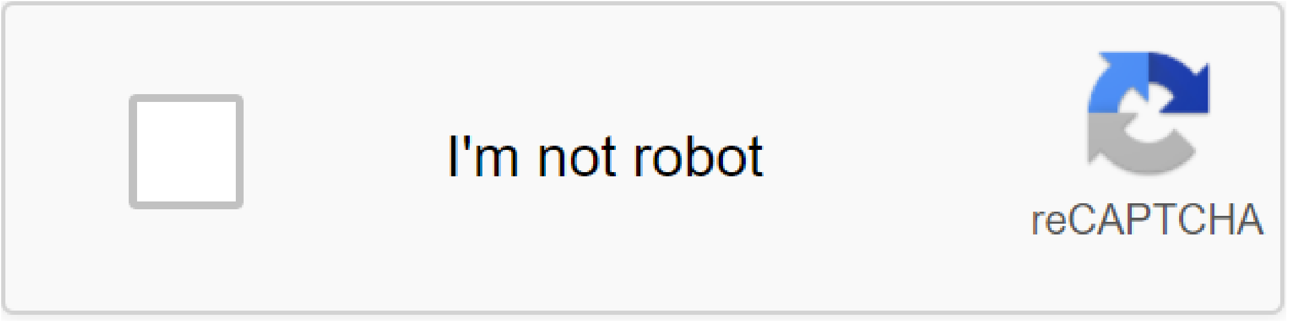
Dspic30f programmer’s reference manual



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Einige Word-Funktionen cuennen in Google Docs nicht angezeigt werden und werden bei nderungen entferntDetails anzeigenLetzte anzeigen This section provides an overview of the 16-bit model of the programmer of the following device families: 16-bit microcontroller (MCU): 16-bit Digital Signal Controllers (DSC): dsPIC30F dsPIC33F dsPIC333E Links are provided on this page for various aspects of the 16-bit architecture set of family instructions (ISA): Memory Organization: Address space (number of seats addressed) Address (how many bits per place) Registers: How many? What size? How are they used? Set of instructions: TIP ISA, data types, instruction categories, address modes, software stack pointer The main reference to this page is the 16-bit MCU and dsPIC® Programmer's Handbook (DS70157). Registers 16-bit basic registers of 16-bit MCU and DSC devices have sixteen 16-bit work registers that are displayed on the memory of the first 16 words in the data memory. Each of the work registers can act as a register of data, addresses, or biases. The 16th Work Register (W15) works like Stack Pointer software for interruptions and calls. In addition, W0-W3 is used to conduct the results of some DIV and MUL operations, as shown at the moment. The following basic registers are also available on all 16-bit devices: CORCON: Used to customize the processor configuration. It provides an opportunity to map the space of the program in the data space. PSVPAG: Used to select a 32 kByte area of the program's memory space that is displayed in the data address space. TBLPAG: Used to hold the top 8-bits of the program's memory address during table reading/writing operations. RCOUNT: Contains a cycle counter for repeat instruction. PCH:PCL: Program counter. Note: The Least Significant Bit (LSb) program counter is always 0 when accessing the instructions. LSb Program Memory Address (PC) is reserved as a bit of choice to access the program's memory from the data space that uses the Space Visibility (PSV) program or table instructions. Instructions only exist in the program's memory space (not configuration space). The program counter uses bits from 0 to 22 only to solve instructions in this space. The most significant bit (MSb) of the program counter (bit 23) will be 1 when accessing data through Table Read or Table Write operations in the configuration space. DSP-Specific Registers Some of the standard work registers have additional functionality for Digital Signal Processor (DSP) operations as shown: In addition, there are several DSP-specific registers, including two 40-bit batteries (A and B) available for DSP operations, as shown: DCOUNT: do-cycle counter for hardware cycles. DOSTART: Contains a starter address for the DO hardware cycle. DOEND: Contains the end of the address for the DO hardware cycle. ACCA/ACCB: 40-bit wide registers used by DSP to perform mathematical and interchangeable operations. For more information about the 16-bit DSP features, go to this page. Instructions Set is an ISA Classification Of CPU types set of architectures can be categorized depending on where operands come from in arithmetic logical units (ALU) operations. There are four main classifications: Stack OP1 Stack OP2 Stack Battery-Memory OP1 Battery OP2 Memory Register Memory-Memory Register OP2 Memory Register (Load/Store) OP1 CPU Registration OP2 CPU Registration Most MCU processors are memory register machines, since memory technology speed often corresponds to processor speed. These architectures support effective bit operations (read/change/write). Today's high-performance MCU processors are increasingly moving to the Load/Store architecture to take processor speeds away from memory speeds and use cache memories to ensure a sustainable high-performance processor. The ISA classification defines the necessary address modes for a set of instructions: the 16-bit ISA PIC24/dsPIC classification implements the hybrid ISA architecture, supporting both The Register and Register, as shown below: In addition, the 40-bit ALU DSP implements the Accumulator-Memory architecture described here. The types of ALU data in 16-bit MCU devices (PIC24F/H/E) support two main types of data: 8-bit two complementary integers. The 16-bit two complements the integers. The 16-bit DSC (dsPICxx) devices support the additional types of DSP data described here. In addition to the ALU, 16-bit MCUs and DSCs include a special 17x17 Hardware multiplier as well as hardware signed/unsigned operations 16/16 and 32/16 Division. The 16-bit instruction set of MCU and DSC instructions provides a rich set of instructions that support traditional microcontroller applications and a class of instructions that support mathematically intensive applications. Most instructions are encoded in a single 24-bit word and run in a single learning cycle. Depending on the device family, the 16-bit set of MCU and DSC instructions contains up to 84 instructions that can be grouped into functional categories shown in the following table: a set of instructions is fully documented in the 16-bit MCU and the DSC Programmer's Handbook (DS70157). The 16-bit MCU and DSC address modes support three native address modes for access to data memory, as well as several forms of immediate solution. Access to the data can be made using the address of the file register, registration of direct or indirect address and immediate circulation, allowing the use of a fixed cost in the instructions. The range of data memory addresses available to each address mode is summed up below: File Register (Memory Direct) File Register (or Memory Direct) address provides the ability to work on data stored in the lower 8 kBytes kBytes (NEAR RAM). Instructions use a predetermined address as an opera. Most of the instructions that use the address register file provide byte/word access to the bottom 8 kBytes of memory data, except for the MOV instruction, which provides access to the word for all 64 kBytes. This allows you to upload data from anywhere in your data memory to any work register (W0:W15) and store the contents of any work register anywhere in your data memory. Examples of access to the File Register are below: a direct register address register is used to access the contents of 16 work registers (W0:W15). Any work register can be used for any instruction that supports this address mode. Instructions using this address mode use the contents of the work register as operands to process the operation. This address mode supports access to both information and word of the word. An example of instructions that use a direct address register is shown below: Registration of indirect address register is used to indirectly access any place in the data memory by treating the contents of the work register as an effective address (EA) to the data memory. Essentially, the contents of the work register become a pointer to the location in the data memory, which should be available by instructions. In addition, the contents of the work register can be changed before or after the operation, providing an effective mechanism for sequential processing of data stored in memory. The modes of indirect circulation supported are shown below: The following examples illustrate the indirect treatment with the pre/post increment/decrement of EA modifications: Immediate treatment In an immediate solution, the coding instruction contains a predetermined permanent operand that is used by the instruction. The amount of work involved varies depending on the type of instruction. 1-bit, 4-bit, 5-bit, 6-bit, 8-bit, 10-bit, 14-bit, and 16-bit constants are allowed, depending on the instruction. Constants may or may not be signed. Below are a few examples using an immediate solution: Software stacks a 16-bit MCU and DSC devices feature software stack that facilitates call and decision processing exceptions. The W15 is the default Stack Pointer (SP). Once reset, it is initialized to 0x0800 (0x1000 for PIC24E and dsPIC33E devices). This ensures that SP points to valid RAM and allows a stack of availability for exceptions that may arise before sp is installed by user software. The user can reprogram SP while initialing anywhere in the data space. SP always points to the first available free word (Top-of-Stack) and stack of software, working from lower addresses to higher addresses. These are preliminary decrements for the POP stack (read) and after increment for the PUSH stack (write). Software stack manipulated by push and POP instructions. PUSH and POP instructions are equivalent to MOV instructions, with W15 used as an destination pointer. For example, W0 content may be pusHed on Top-of-Stack (TOS) by: This syntax is equivalent: TOS content can be returned to W0: This syntax is equivalent: This section describes the increase in ISA EDS, pic24E and dsPIC33E: EDS, referring to the basic address Data Space, is used in conjunction with the reading or writing page register (DSRPAG or DSWPAG) to form EDS addresses that can also be used to access PSV: EDS can be considered as 8 MWords or 16 MBytes. For more information about access to EDS, PSV and table, please refer to Section 3 Data Memory (DS70595) in DsPIC33E/PIC24E Family Reference Manual. Please visit this page to learn more about contacting EDS. Other extensions a number of other extensions have been implemented: Automatic Mixed Multiplication Sign Mode (dsPIC33E) MCU Multiplication with 16-bit result of the hardware stack for DO Loops (dsPIC33E) DSP Context Switch Support (dsPIC33E) Extended CALL and GOTO Instructions New Compare-Branch (CPBxx) Instructions (PIC24E/ds333) browse the 16-bit MCU and programmer's DSC handbook (DS70157). (DS70157)». dspic30f/33f programmer's reference manual

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