Qualcomm hexagon instruction set

The hexagon is the language of the assembly, established in 2006. The Hexagon (DSP6) is a brand for the family of 32-bit multi-thousand microarchitectures, implementing the same set of instructions for the digital signal processor (DSP) developed by Kvalcomm. In 2012, it is estimated that in 2011, the company shipped 1.2 billion DSP cores inside its chip system (SoCs) (an average of 2.3 DSP cores per SoC), and 1.5 billion cores were planned for 2012, that makes DSP6 the most shipped DSP architecture (in 2011, about 1 billion DSP cores were shipped, 90% of the DSP IP license market). The hexagon architecture is designed to provide performance with low power across applications. Find out more about Wikipedia... 14Years Old 1,053Usor? Example jobs code from Wikipedia: - R17:16 - MEMD (R0-M1) MEMD (R6-M1) - R25:24 R20 - CMPY (R20, R8): R13:12) No:endloop0 Last update August 9, 2020 Edit hexagon on GitHub qualifier Technology have developed a hexagonal digital signal processor (DSP) as a world-class processor with processor and DSP functionality to support the deeply embedded needs of the mobile platform processing for multimedia and moder functions. It's an advanced, variable-length instruction, a very long architecture of the Instruction Word (VLIW) processor with multi-thousand hardware. The hexagon architecture and the core family provide Kvalcomm Technologies with a competitive performance and energy efficiency advantage for modem and multifunctional applications and is a key component of all Snapdragon processors™ qualcomm. Шестиугольник Core ArchitectureHexagon 400Hexagon 500Hexagon 600Key AttributesFixed PointFloating PointHexagon Вектор eXtensions (HVX)Премиум Tier801, 805, 808, 810820, 821High Tier602A615, 161, 617, 625, 650, 652Mid Tier410, 412, 415, 430Low Tier208, 210, 212SDK VersionAddOn_600SDK 2.0 SDK 3.0Command Line Tools5.0, 5.15.0, 5.1 , 6.2, 6.47.2, 7.3RTOS'RT'RT'RT'RTRT'RTRT Processor Background: Осенью 2004 г. компания «Квалкомм Технологии» приступила к разработке новой архитектуры процессоров DSP и высокой производительности. In 2011, Hexagon Access was launched to allow customers to program DSP and thus take advantage of the power and performance of unloading ARM cores for performance, reduced power dissipation, or competitive requirements. Since 2012, several hexagonal nuclei have formed a processor behind almost every commercially downloaded 4G LTE modem from Kvalcomm Technologies. The Hexagon DSP core is currently in the 5th generation and integrated into all the latest technology modems and application chips. At Uplinq 2013, we released the first public development environment for Hexagon DSP, Hexagon SDK. Kernel optimized for both high performance and energy efficiency. Energy efficiency is often a more important indicator. A A Pushing performance through MHz, the structures strive for a high level of work per cycle, but at a reduced clock speed. Maintaining a low speed allows implementation to avoid many of the costly design methods that are typical of high-speed construction. One of the problems with thousands is to have a power scale with the number of threads running. Thanks to the carefully orchestrated hierarchical preparation of the watch, the almost perfect scaling of power is achieved. Hexagonal cores use a semi-ordinary physical design methodology with power-reduction settings. Implementations have evolved from simple inter-heavy multi-heavy (IMT) to more advanced priority planning to get the most efficient for planning as many slots as possible to perform. The number of hardware streams has changed over generations to meet the different needs of products and applications. The hexagon V1 initial core supported six streams, but the latest version of the Hexagon DSP, the Hexagon V5, has three streams. For a programmer, these hardware streams can be seen as separate cores of a general memory processor and programmed using regular software streams. The programmer doesn't need to focus on threading, as RTOS software streams maps into hardware processor streams. These hardware threads share the entire memory hierarchy, including L1. Thus, it is very profitable for software to use threads that collaborate on shared data. To facilitate this, the very fast core of RTOS was designed for the hexagon. RTOS globally plans the most prioritized collapsed software streams and always directs interruptions to low-level hardware flows. Unlike most architectures, a set of hexagon instructions originated and evolved, suggesting the existence of a multi-dark implementation. The inherent delay in tolerance afforded to thousands of years has enabled the optimization of the ISA, which would otherwise not be practical. The hexagon goes beyond the usual VLIW and allows you to group both independent and many forms of dependent instructions. For example, a general load comparison idioms can be expressed in one packet of hexagon instructions. Such methods allow you to extract highly concurrency instructions even from irregular control code applications. The ISA has a static grouping of VLIW-style instructions. Multi-pot and VLIW are complementary technologies. Thousands of obscures pipeline latency, which make the instructions of latencies seem low. low instructions allows the compiler to make better use of VLIW packages. The isa hexagon is a hybrid DSP/CPU that has a 4-release VLIW comprised of dual load/shop slots and dual 64-bit performance vector execution All instructions work on a total 32-entry into the thread register file. Vector operations use pairs of registers from the general register. The ISA has a rich set of DSP arithmetic support, including 16-bit and 32-bit fractional and complex data types, a 32-bit floating point and full 64-bit arithmetic support. Competitive data from applications such as H.264, AMR-WB and AAC will be presented. A public description of this architecture was recently presented in 2013 at the Hot Chips conference at Stanford University in August. The processor has been benchmarking with appropriate DSP processors by a leading independent company that analyzes digital signal processors, Berkeley Design Technologies Incorporated (BDTI). The results of this benchmark can be found on the BDTI website. The hexagon hardware processor is a lot of threaded, variable-length instruction, VLIW processor architecture designed to effectively manage and process signal code execution at the low power levels required for mobile platforms. This article may be too technical for most readers to understand. Please help improve it to make it understandable to non-experts without deleting technical details. (March 2016) (Learn how and when to delete this template message) HexagonDesigner'commBits32-bitIntroduced2006 (DSP6)Design4-way multi-national VLIWTypeRegister-RegisterEncodingFixed 4 byte per instruction, Up to 4 instructions in VLIW multiinstructionOpenProprietaryRegistersGeneral purpose32-bit GPR: 32, can be paired with a 64-bit hexagon (DSP6) is a brand for families of 32-bit multi-thousand microarchitectures, implementing the same set of instructions for the digital signal processor (DSP) developed by the company. In 2012, it was estimated that in 2011, the company shipped 1.2 billion DSP cores inside its chip system (SoCs) (an average of 2.3 DSP cores per SoC), and 1.5 billion cores were planned for 2012, that made DSP6 the most shipped DSP architecture (CEVA had about 1 billion DSP cores shipped in 2011, with 90% of the DSP market being recalled to IP license it was shipped). The hexagon architecture is designed to provide performance with low power across applications. It has features such as multi-slack hardware, privilege levels, a very long instructional word (VLIW), a single instruction manual, multiple data (SIMD), and instructions to efficiently process signals. The processor is capable of sending up to 4 instructions (package) up to 4 units of execution each hour. The hardware is multi-thousanded implemented as thousands of barrels - the strands switch in a circular fashion each cycle, so that the 600 MHz physical core is presented as three logical 200 MHz cores to the V5. The V5 hexagon switched to dynamic multi-precision (DMT) with switch L2 misses, interruption of waiting or special special At Hot Chips 2013, the company announced the details of its 680 DSP hexagon. The company announced the expansion of the hexagon vector (HVX). HVX is designed to allow significant computational loads for advanced images and computer vision to be processed on the DSP instead of the processor. In March 2015, the company announced its Snapdragon Neural Processing Engine SDK processor, which allows AI acceleration using processor, GPU and hexagon DSP. The Snapdragon 855 from qualcomm contains a 4th generation AI engine that includes a 690 DSP hexagon and a Tensor Accelerator (HTA) hexagon for AI acceleration. Port Linux software support operating systems for the hexagon run under the Hypervisor (Hexagon Virtual Machine) layer and have been combined with 3.2 kernel release. The original hypervisor is a closed source, and in April 2013, the minimum open source hypervisor implementation for the V2 and V3, the Hexagon MiniVM, was released by Kvalcomm under BSD-style license. The hexagon support compilers were added to the 3.1 release of Tony Linthicum's LLVM. Support for the Hexagon/HVX V66 ISA was added to LLVM 8.0.0. There is also a non-FSF supported affiliate of GCC and Binutils. Since 2006, soC from qualcomm has accessed the SIP-Hexagon DSPs. Modem cores are programmed only to qualcomm, and only the multimedia core can be programmed by the user. They are also used in some of the company's femto-target processors, including FSM98xx, FSM99xx and FSM90xx. In May 2018, WolfSSL added support for the use of the qualcomm hexagon. This is support for launching wolfSSL crypto operations on DSP. In addition to using crypto operations, a specialized operation load management library was later added. Versions released six versions of the architecture: V1 (2006), V2 (2007-2008), V3 (2009), V4 (2010-2011), DSP6 V5 (2013, in Snapdragon 800); and the NODSP6 V6 (2016, in Snapdragon 820). The V4 has 20 DMIPS per milliwatt, operating at 500 MHz. Versions of the DSP6, nm Date, the number of simultaneous streams on the streaming clock, the MHz general core clock, MHz DSP6 V1 65 Production Oct. 2006 DSP6 V2 65 December 2007. 6 100 600 DSP6 V3 (1st gene) 45 2009 6 67 400 DSP6 V3 (2nd gene) 45 2009 2009 4 100 400 DSP6 V4 (V4M, V4C, V4L) 28 2010-2011 3 x 167 500 DSP6 V5 (V5A, V5H) 28 2013 3 600 «DSP6 V6» или 680 »31» 14 2016 4 500 2000 Snapdragon 820/821 682 10 2017 Snapdragon 835 685 10 2018 4'32» Snapdragon 845 6 90 2019 Snapdragon 855/855 698 7 2020 Snapdragon 865/865 Доступность в продуктах Snapdragon Как шестиугольник (DSP6), так и до шестиугольник (DSP5) ядра используются в современных процессорах qualcomm SoCs, qDSP5 в основном в низкопродажных продуктах. Модемные ЦДХП (часто до шестиугольника) не отображаются в таблице. QDSP5 usage: Snapdragon generation Chipset (SoC) ID DSP Generation DSP Frequency, MHz Process node, nm S1[28] MSM7627, MSM7227, MSM7625, MSM7225 QDSP5 320 65 S1[28] MSM7627A, MSM7227A, MSM7625A, MSM7225A QDSP5 350 45 S2[28] MSM8655, MSM8255, APQ8055, MSM7630, MSM7230 QDSP5 256 45 S4 Play[28] MSM8625, MSM8225 QDSP5 350 45 S200[33] 8110, 8210, 8610, 8112, 8212, 8612, 8225Q, 8625Q QDSP5 384 45 LP QDSP6 (Hexagon) usage: Snapdragon generation Chipset (SoC) ID QDSP6 version DSP Frequency, MHz Process node, nm S1[28] QSD8650, QSD8250 QDSP6 600 65 S3[28] MSM8660, MSM8260, APQ8060 QDSP6 (V3?) 400 45 S4 Prime[28] MPQ8064 QDSP6 (V3?) 500 28 S4 Pro[28] MSM8960 Pro, APQ8064 QDSP6 (V3?) 500 28 S4 Plus[28] MSM8960, MSM8660A, MSM8260A , AM38060A, MCM8930, MCM8630, MCM8230, АП38030, MCM8627, MCM8227 ДДСП6 (V3?) 500 28 S400 8926, 8930, 8230, 8630, 8930, 8930, 8930, 8930, 8930AB,AB 8230AB, 8630AB, 8030AB, 8226, 8626 «DSP6V4 500 28 LP S600» 8064T, 8064M «DSP6V4 500 28 LP S80 Поддерживается 8974, 8274, 8674, 8074 xDSP6V5A 600 28 HPm S820 Различные видео кодеки, поддерживаемые Snapdragon SoCs. D - декодирование; E - кодировать FHD и FullHD 1080p 1920x1080px HD и 720p, который может быть 1366x768px или 1280x720px Snapdragon 200 серии Различные видео кодеки поддерживается Snapdragon 200 серии. Кодек Львиный зев 200 (Snapdragon 200) 200 (Квалкомм 205) Львиный зев 208/210 (Snapdragon 212) 2013 2013 2017 2014 2015 Шестиугольник ХДСП5 ХСП6 536 536 X263 Д E H.264 10-битный - - - - - VP8 D - E D - E D - E D - E D - E D - E H.265 D HD - E HD D HD 10-битный - - - H.265 12-битный - - - - VVC VP9 - - - - VP9 10-битный - - - - - AV1 - - - - - - - - Snapdragon 400 серии Различные видео кодеки поддерживается Snapdragon 400 серии. Кодек Львиный зев 400 (Snapdragon 410/415) Snapdragon 425/427 Snapdragon 429/439(439) Snapdragon 450(41) Snapdragon 460 2 квартал 2018 г. - 2 квартал 2017 г.? Шестиугольник NODSP6 ХДСП6 V5? 536 546 683 H263 D E D - E D - E D - E D - E D - E H.265 - D - - - H.265 12-битный - - - - H.265 12-битный - - - - - - - - - - - - - VP9 - - - - - VP9 10-битный - - - - - AV1 - - - - -

- - - Поддержка частоты кадров видео Декодирование HD 60 fps FHD 60 fps FHD 60 fps FHD 60 fps Видео частота кадров HD 60 fps FHD 60 fps FHD 60 fps FHD 60 fps Snapdragon 600 Snapdragon 650/652/653 Snapdragon 630(45) Snapdragon 632(40) Snapdragon 632(40) Snapdragon 636/660 2015. 2 2018 - 2019 - DSP6 V50 (DSP6 V56 642 546 680 685 H263 D)? H.264 D - E D - E D - D? VVC - - - - - - - - VP9 - - D D - E D - E D - E D - E VP9 10-битный - - - - - AV1 - - - - - - - - - - Поддержка частоты видеорамки Декодирование HD 60 fps HD 120 fps HD 240 fps HD 240fps HD 240 fps HD 240 fps HD 240 fps FHD 30 fps FHD 60 fHD 120 fps FHD 120 fps FHD 120 fps FHD 120 fps FHD 120 fps (FHD 120 fps No 4K No 4K 4K30 fps 4K30) 4K30 4K30 fps 4K30 60 fps HD 60 fps HD 240 fps HD 240 fps HD 240 fps HD 240 fps FHD 30 fHD 30 fHD 120 fps FHD 120 fPS FHD 120 fHD 120 fps FHD 120 fps (FHD 120 fps No 4K No 4K 4K30 fps 4K30) 4K30 4K30 fps 4K30 4K60 Others Snapdragon 700 серии Различные видеокодекты Snapdragon 700. Snapdragon 76.5G 5G /765 5G/768G 5G - 685 692 688 696. - E D - E D - E D - E H.264 10-- - - VP8 D - E D - E D - E D - E D 265 10-D - E D - E D - E H.265 12-- - - - VVC - - - - - VP9 D - E D - 'E D' HD 240 fps HD 240 fps HD 240 fps HD 240 fps HD 480 fps FHD 120 fps FHD 120 fps FHD 120 fps FHD 120 fps? FHD 120 fps FHD 120 fps FHD 120 fps FHD 120 fps? 4K 30fps 4K 30fps 4K 30fps? HDR10 HDR10, HLG HDR10 HDR10, HDR10, HLG, Rec. 2020 Snapdragon 800 Кодек Львиный зев 800 (Snapdragon 801) Snapdragon 805(61) Snapdragon 810 (Snapdragon 820/821) Snapdragon 835/855 Snapdragon 845/850(64) Snapdragon 855/855 Наличие No2 2 2013 2014 за 1 квартал 2014 г. 3 квартал 2014 г. 4 квартал 2015 г. 2016 г. 2017 г. 1 2018 г. 2019 г. Шестиугольник «ДДСП6 V5» V56 V56 680 682 685 690 690 698 МПЭГ-4 D - E H263 D - E-69 VC-1 D - E H.264 D H.265 N/A D - E 720P30 D - E H.265 10-битный N/A D D - E VP9 D - E VP9 10-битный D AV1 N/A VVC N/A FHD@240 4K@120 Декодирование FPS HD@120 HD@240 HD@480 HD@960 FHD@60 FHD@120 FHD@240 HD@480 4K@60 8K@30 FPS coding HD@120 HD@240 HD@480 73 HD@480 HD@960 FHD@60 FHD@120 FHD@240 73 FHD@240 4K@120 4K@30 4K@60 73 4K@60 8K@30 other HDR10 Only DECryption HDR10, BT.2020 HLG (HDR10) HDR10 (HDR10) Sample Code This is a single package of instructions from the internal FFT loop: R8): qlt;lt;lt;1:rnd:sat R11:10 - VADDH (R11:10, R13:12) : endloop0 This package is said to be equal to 29 classic OPERATIONS RI; it includes vector addition (4x 16-bit), comprehensive support for the multiplication cycle and hardware cycle. All of the package's instructions are in the same loop. See also the list of qualcomm Snapdragon-on-chip Texas Instruments TMS320 CEVA systems, Inc. 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