Explain instruction format of 8086

1. 8086 INVENT FORMATS, compiled by: L. Krishnananda, Associate Professor, REVA ITM, Bangalore 1 Byte 3 Byte 4 UNIT 2. Instruction format: The sizes of the 8086 instructions range from one to six bytes. Depending on the type of coding, the instruction may have more than one Hexcode (not as unique as in 8085) the OP code field takes 6 bits. It identifies an operation that must be performed according to the instructions. Registration direct bit (D) takes one bit. It determines whether the operand of the register in byte two is the source or the operand of the destination. D-1 indicates that the operand register is an operand destination. D-0 indicates that the register is the source. A bit of data size (W) determines whether the operation that will be performed 8 bits or 16 bits of data, W-0 points to the 8-bit W'1 operation, pointing to a 16-bit operation 7 2 1 1 0 7 6 6 5 4 3 2 1 1 0 Opcode D W MOD REG R/M Low Disp/DATA High Disp/DATA Second stroke and the instructions usually determine whether one of the operands is in or both are registers. This range contains three fields. This is the mode field (MOD), register field (REG) and Register/Memory field (R/M). MOD Mode (2 bits) Interpretation 00 Memory without displacement follows except for 16 bit bias, when R/M-110 01 Memory Mode with 8-bit offset 10 Memory mode with 16 bit offset 11 Register mode (without bias) Register field takes 3 bits. It identifies the register for the first opera, which is listed as the source or destination of bit D. Registration codes: Byte 1 Byte 2 OR Register Operand/Register for use EA Calculation Register Operand/Extension opcode Register/Memory mode with Word/byte operation Direction travel length is registration/from operation code DIRECT ADDRESS LOW ADDRESS ADDRESS HIGH. 8086 INSTRUCTION FORMATS Compiled: L. Krishnananda, Associate Professor, REVA ITM, Bangalore 2 REG W'0 W'000 AL AX 001 CL CX 010 DL DX 011 BL BX 100 AH SP 101 CH BP 110 DH SI 111TH FIELD DI R/M takes 3 bits. The R/M field, along with the MOD field, identifies the second operand, as shown below. MOD 11 R/M W'0 W'1 000 AL AX 001 CL CX 010 DL DX 011 BL BX 100 AH SP 101 CH BP 110 DH SI 111 BH DI Effective calculation of R/M MOD-address 00 MOD 00 MOD 110 DH SI 111 BH DI Effective calculation address R/M MOD 01 MOD 10,000 (BX) (SI) (SI) (SI)-D8 (BX) (SI)-D16 001 (BX) (DI) (BX) (DI) BP) (SI) (BP) (BP) (SI) (SI) (SI) (SI) (SI) (SI) 016 011 (D) (DI) (DI) (DI)1 (DI) (DI) (DI) (DI)) - D8 (DI) - D16 110 Direct Address (BP) - D8 (BP) - D16 111 (BX) (BX) - D8 (BX) - D16 In the aforementioned R/M field coding depends on how the mode field is installed. If MOD-11 (register in registration mode), this R/M identifies the second register. MOD selects the memory mode, then R/M shows how the effective address of the operand memory is calculated. Bytes 3 to 6 instructions are additional fields that MOD/R/M Memory (EA) Registration Mode 00 01 10 VT-0 W-1 000 (BX) (SI) (BX) (SI) (BX) (DI) 011 (BP) (BP) (BP) (BP) (DI) d8 (DI) - d16 CH BP 110 d16 (BP) 8086 FORMAT INSTRUCTIONS Compiled: L. Krishnananda, Associate Professor, REVA ITM, Bangalore 3 usually contain the value of moving operand memory and/or the actual value of the immediate constant operand. Get opcodes for the following instructions. Example 1 : Code for MOV CH, BL This instruction transmits 8 bit BL content in CH 6 bit Opcode for this instruction 1000102 D bit indicates whether the register specified by the REG byte 2 field is the source or destination of the operand. D-0 indicates that BL is the source of operand. Operation B-0 byte B byte 2, since the second operand register mod field 112. Field R/M No. 101 (CH) Register (REG) field No. 011 (BL) Hence the machine code for MOV CH, BL 10001000 11 011 101 Byte 1 Byte2 and 88DDH Sample 2: Code for SUB BX, (DI) This instruction subtract 16-bit memory content addressed to DI and DX from BX. 6-bit Opcode for SUB 0010102. The D-1 is so that the REG byte 2 field is the destination of the operand. W-1 indicates a 16-bit operation. MOD No 00 REG 011 R/M 101 Machine code 0010 1011 0001 1101 2 B 1 D Sample 3:Code for MOV 1234 (BP), DX Here we pointed out DX using the REG field, D bit should be 0, indicating DX is the original register. The REG field should be 010 to indicate the DX register. The W bit should be one to indicate that it is a word operation. 1234 BP is indicated using MOD 10 and R/M values 110 and offsets 1234H. The 4th code for this instruction will be 89 96 34 12H. Opcode D W MOD REG R/M LB displacement HB move 100010 0 1 10 010 110 34H 12H Sample 4:Code for MOV DS : 2345 BP DX Here we have to point DX using the field. Bit D should be 0, indicating that Dx is the original register. The REG field should be 010 to indicate the DX register. The W bit should be one to indicate that it is a word operation. 2345 BP is listed with MOD-10 and R/M No. 110 and moving 2345 H. Whenever BP is used to create an effective address (EA), the default segment will be SS. In this example, we want the segment register to be the DS we have to provide 4. 8086 INSTRUCTION FORMATS Compiled by: L. Krishnananda, Associate Professor, REVA ITM, Bangalore 4 Segment to redefine byte consoles (SOP byte) to begin with. Byte SOP is 001 xx 110, where the SR value is provided according to the table shown below. xx Register Segment 00 ES 01 CS 10 SS 11 DS To indicate the DS register, the SOP honeycomb will be 001 11 110 and 3E H. So the 5th code for this instruction will be 3E 89 96 23 H. SOP Opcode D W MOD REG R/M LB disp. HD disp. 3EH 1000 10 0 1 10 010 110 45 23 Suppose we want to code MOV SS : 2345 (BP), DX. This generates only the 4th code, without SOP byte, since SS is already the default segment register in this case. Example 5: Give the instruction template and create a code for ADD 0FABE (BX), DI, DX (add 0000000) ADD 0FABE (BX) and DX Here we have to specify DX using the REG field. Bit D 0, which indicates that DX is the original register. The REG field should be 010 to indicate the DX register. W should be one to indicate that this is the word operation. FABE (BX and DI) is indicated using MOD 10 and R/M 001 (from the composite table). The 4th code for this instruction will be Opcode D W MOD REG R/M 16 bit disp. 000000 0 1 10 010 001 BEH FAH No 01 91 BE FAH Example 6 : Give the template instructions and create a code for the MOV AX instruction, BX (MOV instruction code - 100010) is the AX destination register with D-1, and the code for AX is 000 BX using 00 Mode and R/M 111. This is the word opcode D W Mod REG R/M 100010 1 1 1 000 111 No8B 07H INPUT/OUTPUT INSTRUCTIONS: IN acc, port : In the transfer of a tote or word from the port of entry to the AL register or register AX, respectively. My port number will be listed either with an immediate permanent map, allowing you to access ports with a number of 0 to 255 or with a number previously placed in the DX register allowing variable access (by changing the value in DX) to ports numbered from 0 to 65,535. In Operands Example acc, immB In AL, 0E2H (OR) in AX, PORT acc, DX in AX, DX (OR) in AL, DX 5. 8086 INSTRUCTION FORMATS Compiled by L. Krishnananda, Associate Professor, REVA ITM, Bangalore 5 OUT Port, acc : Out transmits byte or word from the AL or AX register respectively to the severance port. Port numbers can be listed either immediately or with a number previously placed in the DX register allowing variable access. Flags are not affected. In Operands Example Imm 8, acc OUT 32, AX (OR) OUT PORT, AL DX, acc OUT DX, AL (OR) OUT DX, AX I/O Mode (straight) : Port number 8 bit immediate operand. Example : OUT 05 H, AL Outputs (AL) to 8-bit port 05 H I/O (indirect): port number taken from DX. Example 1 : INAL, DX If the contents of 5040 8 bits in port 5040 moves to AL. Example 2 : IN AX, DX Entrances 8 bit contents of ports 5040 and 5041 in AL and AH respectively. 8086 Instruction 8086 Instruction Format range from 1 to 6 bytes in length. Fig. 6.8 shows the instructions formats for instructions from 1 to 6 bytes. As shown in the pic. 6.8, travel and operandi can be either 8-bit or 16-bit long depending on the instruction. The opcode and address mode are shown using the first two bytes of the instruction. Byte (s) rim/address mode may : There is no additional byte Two byte EA (direct treatment only). One or two byte move One or two byte immediate operand One or two byte moves followed by one or two byte immediate operatic two tote moving and two byte segment address (for direct intersegment solutions only). Most opcodes in 8086 have special 1-bit points. They : W-bit : Some instructions 8086 can work on byte or word. The W-bits in the opcode of this instruction indicate whether the instruction is a series instruction (W No. 0) or a word instruction (W No. 1). D-bit: The D-bit in the instruction op code indicates that the register specified in the instruction is the original register (D No. 0) or the destination register (D No.1). S-bit : 8-bit 2 in addition number can be extended to 16-bit 2 in addition number by making all bits in a higher order byte equal to the most significant bit in a low-order byte. This is known as the extension of the sign. S-bits along with W-bits indicate: V-bit : V-bit solves the number of shifts for rotation and change of instructions. If V No. 0, consider No 1; if V No. 1, the account is in the CL register. For example, if V No. 1 and CL No. 2 then shift or rotate the instructions change or rotate a 2-bit bit: It is used for a string of primitives, such as the REP to compare with the SF flag. (See app A for instruction formats) As seen from the pic. 6.8, if the instruction has two opcode/address bytes, then the second byte is one of the following two forms. where the Mod, Reg and R/M fields indicate the operand described in the following tables. Table. explain instruction format of 8086 with an example. explain the mov instruction encoding format of 8086. explain the mov instruction encoding format of 8086 with a neat sketch