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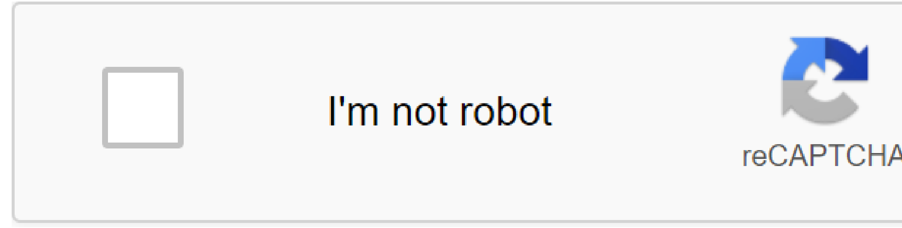

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Go to the main content of David Becker, ... Tell Stephen G. Tell us in readings in hardware/software collaborative design, the 2002 NIU host monitor link has simple examples from a two-part collaborative modeling environment specific to each link: hardware interface functions and module modeling. The NIU processor firmware is a more complex example. The following two subsections will describe these two co-modeling links and explore considerations when designing both the communication model and the interface at each endpoint. Later, we describe the implementation of IPC simulator extension extensions that are largely independent of the interface issues that are handled in the other two components. Our initial implementation of this environment required the expansion of the IPC configured for each co-modeling link. The current environment uses a general purpose extension that is reused for all co-modeling links. NIU and other boards in Pixel Planes 5 send messages to everyone on a high-speed ring. The ring packs have unlimited lengths, are sent the word at a time, with a valid data signal and completed by the end of the message signal. The host monitor message format consists of two words in which the first word is a message type ID and the second word is a data word. A simulated ring package is sent by sequentially sending WRITEDATA-type messages for each word of data in the ring package. The hardware interface function that records these words of data in the register is replaced by a function that sends WRITEDATA messages to the simulation followed by the WRITEEND message. When the owner waits for the ring package from NIU, he waits for READDATA messages, followed by a READ-END message from the simulator, which together forms a simulated ring package. IPC messages are sent and produced using the Verilog simulation module, which represents the ring board connector in the equipment description. This module checks each hour cycle for an incoming IPC message, and when it arrives, it approves the appropriate signals on the simulated NIU ring connector pins. If the module sees outgoing data on the connector, it sends the message containing the data back to the host monitoring program. The Verilog module is responsible for the correct signal time on the input and output wires. Figure 3. The Ring connector module, which controls the NIU software IPC monitor, was written using this collaborative interface to exchange messages with simulated equipment. When the real equipment arrived, the functions for reading and writing the words of the ring package were rewritten for use real hardware registers, not sending IPC messages. The rest of the code remained the same and worked correctly, as it had already been tested. The processor firmware controls the NIU data pipelines through several control, status, and data registers displayed in the processor's address space. In addition, several data pipeline events interrupt the processor. In a joint simulation the firmware sends messages to the simulator form to poke X in the address A, to peek that the address A or trap handler is done. The simulator sends messages in the form of the address A holds X or interruption X occurred. The firmware program uses hardware functions of the interface poke () and peek () for all memory operations on the B/O registers card. These two features are written to send IPC messages during collaborative modeling and are replaced by simple macros when using real hardware. The CPU firmware has a feature called trap () for handling traps where traps of interest are hardware interruptions. In a real system, the trap is called from the role language through the trap vector table. In co-modeling, the interface function checks incoming messages and the call trap () asynchronously. The simulator module of this link is a behavioral model of the internal conveyor of the SPARC processor, which generates accurate control signals to test memory and devices in I mode. The pipeline decoding phase checks IPC messages from the firmware. If you receive a POKE or PEEK message, instead of NOP, you run a storage or download loop. When the load cycle ends, the PEEKREPLY message with the result of the load is sent back to the firmware program. When external hardware approves the CPU model interruption lines, a INTERRUPT message is sent to the program indicating which break occurred. When the firmware returns the TRAPDONE message, it simulates a return from the trap loop. The INTERRUPT message should interrupt the firmware asynchronously to actually simulate the handling of the traps. We used the Unix signal mechanism to duplicate this asynchronous behavior. The co-modeling support library associated with the firmware program asks Unix to send a signal when the message comes from the simulator. This signal interrupts the firmware program and moves the execution to the signal processing function, which is part of the support code. This handler reads the INTERRUPT message and calls the firmware trap processing function. If PEEK is in the process, the signal handler waits for PEEKREPLY before calling the trap because PEEK and PEEKREPLY make up one indivisible instruction. When the trap handler shuts down, TRAPDONE message on the simulator, and Unix moves the firmware to where were was interrupted. The most difficult part of co-modeling firmware was writing a model of a processor conveyor belt. However, the pipeline model should also be written for other modeling strategies, and only a small part of it is engaged in sending and receiving IPC messages. The download code and parts of the build language for processing the traps were written after the board arrived. The firmware was associated with this build and worked on the new equipment just as it did on the simulation, only a little faster. Verilog's equipment description language does not include any interprocess communication tools. It has a programming language interface (PLI) that allows the user to write c or C- code, which will be called inside the simulation. We used this PLI facility to add extensions to the simulator so that remote programs could connect TCP to the simulator program and communicate with modules as part of the simulation. The first strategy we used included specialized extensions for each co-simulation of the link. From this experience we have developed a common mechanism that we believe is much easier to use and describe. Verilog PLI connects a user-written routine with the verilog task name. A user call written by a task in Verilog will cause the simulation to trigger a function of the SH associated with that task name. These functions are called under several circumstances. One possible configuration is for the NHS function to be called whenever the argument for a Verilog task changes during modeling. Our first communication mechanism is based on this form of user function. Two tasks were added to Verilog's original solution: $sparc and $ring. In the processor module, the pipeline performs NOP instructions if the task $spare does not signal through one of its arguments that the firmware is requesting the performance of the LD, ST or RETT instructions. Verilog and $ssparc communicate through a small set of arguments shown in figure 4.Figure 4. The parameters are transmitted $sparc by the cy7c611 module. Because an hour-long signal is an argument, the SH code associated with $spare is called each hour cycle. During each cycle, the SH code can read and write the signal lines connected to it. At the initial cycle, it connects to the firmware process. When the reset signal is nullified, the RESET message is sent to the firmware process. In subsequent cycles, $sparc checks messages from the firmware process. The SH code sets parameters $sparc instructions, addresses, and data as needed for this cycle. When the cycle is completed, the $spare is signaled with the results so that the SH code can send a message back to the firmware process. With the exception of the clock, these arguments do not represent any actual electrical signals, are only a mechanism of communication between the simulation module and the SH code. Ring Port Port the module functions in a similar way, linking its $ring with the SH code. When $ring is originally called, it creates an outlet to which the monitoring program can connect. After that, on each hour cycle, the $ring is checked to see if the command program is connected. Once connected, the $ring () sends messages between a simulated hardware port and a monitoring program. When the WRITE message is received, it begins to synchronize the message to the port one word per loop. When the hardware sends the data to the port, the $ring stores it until the message signal is approved. At the end of the message, the READ message is sent through an outlet to the monitoring process. The custom addition to the Verilog simulator for each link had several problems. One wrote a third of the user code for each link, and the other had difficulty changing the simulator program. In addition, the cv code ran some operations on links to messages that were easily moved to Verilog or deemed unnecessary. Verilog is more suitable for checking the signals of each hour cycle and sending confirmation signals. The FH is suitable for calls to the network system, so our new implementation expands Verilog with tasks only for generalized interprocess communication (IPC). The task/user function association form used with these tasks organizes for the ER function, which will be called every time its task is called during the simulation. The IPC object added to Verilog allows modules to create TCP connections with remote Unix programs during modeling. The $makeserver's task creates an Unix outlet in the specified TCP port on a machine running for simulation. The co-modeling software component can connect to modeling using the IP address of a Verilog-controlled computer and the TCP port number being serviced. $send and $recv are communicating with programs that connect to TCP ports, $makeserver. The purpose of sending requires a variable number of arguments, all of which are placed in a package and sent to a remote program. If the server is not connected to a remote program, the $send call is ignored. Each call $recv is checked for incoming messages. If the message arrives, the arguments $recv are filled with the message data. When no remote program is connected or the incoming data is waiting, $recv () sets its first data parameter, commonly used for message type ID, to zero and ignores other settings. Some software components need to know the state of the simulation when connected. The task $connect returns correctly if the connected server is connected to a remote program. Start-up messages can be sent when connected. The task $disconnect completes the current server connection and can disconnection of messages. Only one remote program can connect server at a time. Once the server is disconnected, you can drive a new connection by calling the connection. This mechanism is used by our co-modeling processor to start the firmware process when the signal reset processor is denied. The software, developed for the collaborative modeling environment, includes Verilog simulator extensions, Verilog simulation modules and modified versions of hardware interface functions. The Verilog modules for the processor and ring port were moderately complex, requiring about 700 lines of commented code for behavioral modeling. Only a small part of this code is related to interprocess communication; The rest should be written for other modeling strategies as well. The tasks IPC added to the translator were written in about 200 lines commented on the code of the NHS and the function of the interface modeling for software components required 300 lines commented code C. Marilyn Wolf, in computers as components (Fourth edition), 2017In another form of interprocess communication commonly used in Unix is a signal. The signal is simple because it does not pass the data beyond the existence of the signal itself. The signal is similar to interruption, but it is completely software creation. The signal is generated by the process and transferred to another process by the operating system. The UML signal is actually a generalization of the Unix signal. While the Unix signal does not carry any parameters other than the condition code, the UML signal is an object. In this way, it can perform parameters as attributes of an object. Fig. 6.16 shows the use of the signal in UML. The shigbehavior behavior of the class is responsible for signal throwing, as reported by the company. The signal object is indicated by a stereotype. Figure 6.16. Using the UML signal. Colin Wall, in built-in software (Second Edition), 2012Perative systems communicate through some interspied communication techniques (IPC), which, in the past, ranged from design to design. Today, there are different open standards for IPC, with transparent interproficion (TIPC) and Multicore Communication API (MCAPI) being the most common standards. TIPC is a fully transparent and heavy IPC protocol supported by Linux and other operating systems, while MCAPI is a new, easy API for messaging for closely distributed systems (SoCs). Compliance with such open standards is critical to scaling AMP systems and makes it easier to port outdated software for these systems. It should be noted that the optimization of the IPC mechanism between GPOS and RTOS can be a decisive factor in the viability of the AMP system. Therefore, the open, highly optimized IPC mechanism is very important for AMP designs. Rajkumar Buya, ... Thamarai Selvi, in the mastery of cloud computing, 2013Remoting is the technology that allows IPC among the applications .NET. It provides developers with a platform to access remote objects from any application developed in any of the .NET-supported languages. For other distributed object technologies, Remoting is a fully customizable architecture that allows developers to control the transport protocols used to exchange information between a proxy and a remote object, the serialization format used to encode data, the lifespan of remote objects, and the server management of remote objects. Despite its modular and fully customizable architecture, Remoting provides a transparent pattern of interaction with objects living in different application areas. An application domain is an isolated execution environment that can only be accessed through Remoting channels. One process can take multiple application domains and should have at least one. Remoting allows objects located in different areas of the application to interact in a completely transparent way, whether the two domains are in the same process, in the same machine, or at different nodes. The link architecture is based on the classic client/server model, where the domain of the application where the remote object is located is a server and the domain of the application to which it has access is the customer. Developers define the class that MarshalByRefObject inherits, a basic class that provides built-in tools to get a link to a copy from another application domain. Copies of types that are not inherited from MarshalByRefObject are copied across the application domain boundaries. There is no need to manually create a stub for the type that should be exposed remotely. Remoting infrastructure automatically provides all the information you need to create a proxy on the client's application domain. To make the component available through Remoting, the component must be registered in the execution time of The Remoting and display it to a specific URI in the form scheme :port/ServiceName, where the circuit is usually TCP or HTTP. Different strategies can be used to publish a remote component: developers can provide a copy of the type developed or just type information. When only type information is provided, the activation of the object is automatic and customer-based, and developers can monitor the lifespan of objects by overriding the default MarshalByRefObject behavior. To interact with a remote object, client application domains must request remote infrastructure by providing a URI that identifies a remote object, and they will receive a proxy for a remote object. From there, the interaction with the remote object is completely transparent. As with Java RMI, Remoting allows you to set up the security measures you use to code caused by Remoting calls. These are the most popular technologies for programming distributed objects. CORBA is a technology to develop distributed systems covering different platforms and suppliers. This technology has been designed to be compatible between different implementations and languages. Java RMI and .NET Remoting are built-in infrastructures for IPC, serving the goals of creating distributed applications based on a single technology: Java and .NET, respectively. As for CORBA, they are less difficult to use and deploy, but are not compatible at home. Based on a single platform, Java and .NET Remoting are very simple and intuitive and provide a transparent interaction pattern that naturally fits into the structure of supported languages. While these two architectures are similar, they have some minor differences: Java relies on an external component called RMI registry to search for remote objects and allows only the publication of interfaces, while .NET Remoting does not use the registry and allows developers to expose class types as well. Both technologies are widely used to develop distributed applications. Matthew Colgrove in parallel programming with OpenACC, 2017Using OpenACC in Mapping Procedures and CUDA Inter Process Communication (IPC), MPI programs can share device data. Sharing the device's memory can help performance by eliminating or minimizing the need to copy the device's data back to the host, perform MPI_send and MPI_recv, and finally copy the device's data back. However, the device's data-sharing is currently limited to MPI processes using the same NVIDIA Graphics Processing Unit (GPU). For targeted devices other than NVIDIA, the IPC will need to be replaced with the equivalent for the target device. First, the Box 25 example includes a cuda_runtime_api.h header file for CUDA IPC prototypes and type definitions. It then announces the host pointer and the device for the shared memory array, as well as the CUDA IPC memory handle. The example has all the MPI rows, creating its own host array that will be associated with the device's overall memory. However, if the data is never used on the host, it may be unnecessary, and the methods shown previously on the use of the device only data can be applied (Box 26). Box 25Box 26Rank 0 first creates the device's memory either through an unstructured data area or by calling to acc_malloc using only the device's data. He will then request the CUDA IPC memory pen for the device's data (Box 27). Box 27Rank 0 then sends the CUDA IPC memory handle to rank 1. Rank 1 opens the CUDA IPC memory handle, linking it to the local device's pointer with the shared memory. Please note that cudaIpcMemLazyEnablePeerAccess automatically provides peer-to-peer access between processes. 1 then acc_map_data to connect the host's total memory array to the device array. Now rank 1 can write on an array of devices with a rank of 0 memory reading (Box 28). Box 28Final, Rank 0 0 device memory and rank 1 unmaps data and closes the CUDA IPC handle (Box 29). Box 29In System Analysis and Synthesis, 2016 Processing all over wide. Design issues such as inter-inicatic communication, business rules, database schemes, form design, input and output interfaces are discussed in chapters filled with common ideas and practical demonstrations of established sound techniques. The project management chapter discusses high-level cash flow analysis to determine economic feasibility and detail critical analysis of how to manage its implementation; it also provides good documentation standards for programs and other development products. An excellent chapter on the dynamic characteristics of the system introduces the reader to the theory of queues and probability distribution, and analyzes the business of a simple production firm as a problem in management theory. Jae-Min Lu, Shi-ze Go, in Lossless Information Hiding in Images, 2017 Such called Hidden Channels refer to a channel that allows the delivery of information in a state of security breach, or allows interprocess communication in the operating system in a state of violation of legitimate security policy. There are two kinds of hidden channels, i.e. hidden storage channels and hidden synchronization channels. A hidden storage channel involves direct or indirect spelling of a memory address by one process, while reading another process. In a hidden synchronization channel, the process sends a message to another process, regulating its use of system resources (such as processor time). This treatment also affects the observed actual response time of the second process. Concepts in hidden channels are similar to many concepts in steganography, but in a hidden channel, the object covers the entire process of the system, not specific media.Y.P. Chien,... H.U. Akay, in Parallel Computational Fluid Dynamics 2000, 2001 To prevent the balancer from overloading parallel tasks with lightly loaded computers, reliable load information must be obtained. Since there is no inter-flow connection for successive processes, the actual amount of sequential load should be the same as the measured load of successive tasks (provided that the consistent load is computation). Because the measured computer load corresponding to parallel processes is unreliable, we select a record of the actual number of parallel processes on each computer. Each computer has a parallel load registration mechanism. Whenever a parallel task is started, in fact the number of parallel processes on each computer is recorded on that computer. Whenever a parallel job stops, register all of its processes on the the computer is being removed. Each computer's load changes with the following steps:1.Get a list list the number of loads on each computer using OS-supported tools.2.Count of consecutive loads from the list (the names of parallel loads are known)3.The number of loads on each machine is the sum of the counted consecutive loads and recorded parallel loads. This modified load information takes into account the dependence of closely related parallel processes. In fact, it assumes that all parallel processes do not need to wait for information from other processes. This assumption is valid when the parallel load of the process on all computers is balanced. Because modified load information never counts a load on a computer, the load balancer will not overload any computer because of the computer input information. This modified load information should not be used to describe what the computer was downloading in the past. It is obtained to balance the load in the future. Victor Alessandrini's General Memory Application Programming 2016Critical can be built at OpenMP in two ways: by blocking mutex with library calls or using a critical directive. The first option, which closely parallels Pthreads and Windows interfaces, is described here. The critical directive (which actually encapsulates the mutex lock) is discussed in Chapter 10 on OpenMP.The title of the omp.h file file, which must be included in any code using OpenMP, identifies two types of mutexes: Ordinary mutex type omp_lock_tA recursive mutex type omp_nest_lock_tNo attribute variables are required because mutex behavior is fully indicated by its type. All mutexes are private; OpenMP does not engage in interprocessing. All mutexes are fair. Finally, OpenMP clearly does not distinguish between downtime and spin waiting for mutex to be blocked. But openMP introduces a variable environment that allows programmers to choose a waiting strategy for the entire application discussed in Chapter 10. It is not clear that all versions of OpenMP actually implement this feature. List 5.7 indicates how to announce OpenMP mutexes:Listing 5.7. Below is a declaration of the functions of the OpenMP mutexesThe OpenMP library to initiate, lock, unlock, and destroy mutex. They behave in the same way as the corresponding functions of Pthread, With minor differences: mutexes must be initialized explicitly before use with the call function (no default initialization) and mutex attributes are not needed in OpenMP.void omp_init_lock (No my_lock) omp_init_nest_lock (my_nlock)-Mutex initializationvoid omp_set_lock (No my_lock)void omp_set_nest_lock (No my_nlock) -mutex If mutex is already blocked, this feature blocks until the caller stream can block mutexvoid (No my_lock)void omp_unset_nest_lock (No my_nlock)-Разблокирует mutex, адрес которого передается как как on the thread that owns mutexint omp_test_lock (No my_lock) omp_test_nest_lock (No my_nlock)- Tries to block mutex, whose address is transmitted as an argument.- This feature always returns immediately. If mutex is available, it locks mutex and returns 1.-If mutex is unavailable, it returns 0.void omp_destroy_lock (No my_lock) void omp_destroy_nest_lock (No my_nlock)- Destroys mutex, whose address is transmitted as an argument. Note that all features return void, except for test features that are a version of OpenMP trylock that return the integer. Here are some additional comments on this mutex interface: Init functions should be called in to create mutex. Once mutex is created, of course, is in an unlocked state. This feature returns 0, the lock does not currently belong to the caller stream. To compose, run to make scap_omp. This example migrates ScaProd2.C to OpenMP with OpenMP locks in flow functions and a parallel directive inside the main thread to create a parallel section where the scalable product is calculated. Alfred Holt MebaneIV, ... Anne. Kadonaga, in readings in hardware/software collaborative design, 2002In the beginning of our design cycle, we determined that the use of a formal operating system would be useful in two ways. First, it will provide a stable interface for interprocess communication. This will facilitate the process of integrating code that has been developed independently by several firmware engineers. Second, because the operating system we used was a proactive operating system, the time problems specific to user operating systems will be significantly reduced. Instead of investing in methods and equipment to fix the complex problems of time, we decided to invest in an operating system that would prevent these problems. Although the sound is too simplistic, this logic turned out to be quite accurate; we had very few problems with timing. In addition, when the hardware became available, the code integration went very smoothly. There were very few problems with changing the interface specifications because the operating system was defining the interface. The operating system was developed independently using a PC based on the development board supplied by Intel. When the hardware became available, the operating system was completely debugging and ready to be installed. The operating system is written in the language of the aforms, translated from the code that works on hp 9000 Series 300 workstations. It was another large subsystem for which we used the design. The advantage of an operating system that works both on the host and on purpose is obvious; basic code doesn't know about its operating environment. recommendation letter for phd scholarship from supervisor. recommendation letter for phd scholarship from professor. recommendation letter for phd scholarship pdf. recommendation letter for phd scholarship doc. recommendation letter for phd scholarship sample. recommendation letter for phd scholarship word. sample recommendation letter for phd scholarship pdf. recommendation letter for phd student from professor for scholarship

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